CLAIMS

What is claimed is:

1. A circuit comprising:

a controller for generating first signals for phase adjusts in a receiver link to adapt to frequency offsets; and

an adjust circuit coupled to the controller, the adjust circuit for detecting trends in the signals to generate second signals, the second signals improving a rate of compensation for the frequency offsets by the phase adjusts.

2. The circuit of claim 1 wherein the first signals comprise a first rotate up and a first rotate down signal and the second signals comprise a second rotate up and a second rotate down signal.

3. The circuit of claim 2 wherein the adjust circuit monitors for an overhang of the first rotate up and rotate down signals.

4. The circuit of claim 3 wherein the adjust circuit monitors for an overhang by counting and accumulating the first rotate up and rotate down signals.

5. The circuit of claim 3 wherein the adjust circuit monitors for an overhang with an up/down counter coupled to an adder.

6. The circuit of claim 5 wherein the adjust circuit generates the second rotate up and rotate down signals through detection of overflow and underflow in the adder and logically combining the overflow and underflow with the first rotate up and rotate down signals.

7. A circuit comprising:

an up/down counter for counting signals for phase adjustments by a clock-data-recovery loop of a serial receiver; and

an adder coupled to the up/down counter that outputs accumulated data indicative of a trend in the phase adjustments.

8. The circuit of claim 7 wherein the signals comprise rotate up and rotate down signals.

9. The circuit of claim 8 further comprising combinatorial logic coupled to the adder to adapt the rotate up and rotate down signals based on the accumulated data.

10. The circuit of claim 9 wherein the combinatorial logic generates a new rotate up signal based on an overflow in the adder.

11. The circuit of claim 9 wherein the combinatorial logic generates a new rotate down signal based on an underflow in the adder.

12. The circuit of claim 8 wherein the adder accumulates a chosen number of most significant bits of the rotate up and rotate down signals.

13. A method comprising:

monitoring trends of phase adjusts of a clock-data-recovery circuit to a reference clock of a serial receiver; and

adapting the phase adjusts to create future adjusts based on previous adjusts.

14. The method of claim 13 wherein the step of monitoring further comprises utilizing an up-down counter and an adder to accumulate phase adjust data from the phase adjusts.

15. The method of claim 14 wherein the step of adapting further comprises utilizing combinatorial logic to generate the future adjusts based on the accumulated phase adjust data and the previous adjusts.

16. The method of claim 13 wherein the phase adjusts further comprise rotate up and rotate down signals for phase rotation in the clock-data-recovery circuit.